Design and Real-Time Implementation of Data-Driven Adaptive Wide-Area Damping Controller for Back-to-back VSC-HVDC

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Abstract

This paper proposes a data-driven adaptive wide-area damping controller (D-WADC) for back-to-back VSC-HVDC to suppress the low frequency oscillation in a large-scale interconnected power system. The proposed D-WADC adopts a dual-loop control structure to make full use of the active and reactive power control of VSC-HVDC to improve the damping of the power system. A data-driven algorithm named the goal representation heuristic dynamic programming is employed to design the proposed D-WADC, which means the design procedure only requires the input and output data rather than the mathematic model of the concerned power system. Thus, the D-WADC can adapt to the change of operating condition through online weight modification. Besides, the adaptive delay compensator (ADC) is added to effectively compensate the stochastic delay involved in the wide-area feedback signal. Case studies are conducted based on the simplified model of a practical power system and the 16-machine system with a back-to-back VSC-HVDC. Both the simulation and hardware-in-loop experiment results verify that the proposed D-WADC can effectively suppress the low-frequency oscillation under a wide range of operating conditions, disturbances, and stochastic communication delays.

Keywords: Wide-area damping controller, VSC-HVDC, goal representation heuristic dynamic programming (GrHDP), adaptive delay compensation, low frequency oscillation.

1. Introduction

High voltage direct current (HVDC) system becomes one of the key technologies for transferring bulk power over a long distance and integrating renewable energy [1]. Compared with the conventional HVDC, the voltage source converter HVDC (VSC-HVDC) has the advantages of no commutation failure, no reactive power compensation problem and independent control of active and reactive power [2, 3, 4, 5]. Furthermore, the back-to-back VSC-HVDC (BTB-VSC-HVDC) can realize the interconnection of two asynchronous AC grid [6, 7], which avoids cascaded failures resulting in blackouts and eliminates part of inter-area oscillations. However, it will lead to the decline of inertia and may weaken the damping of alternating current (AC) grids. The conventional power system stabilizer (PSS) deployed on generators can significantly improve the damping of local oscillations, but may not effective for damping the inter-area oscillations [8]. The reason is that the PSS uses the local measurement as input signal, which usually has low observability of the inter-area oscillations. With the deployment of the wide-area measure system (WAMS), the wide-area measurements with high observability of the inter-area oscillations are available for the wide-area damping controller (WADC) [9, 10, 11, 12]. And, the WADC reasonably designed for BTB-VSC-HVDC can effectively suppress the inter-area low frequency oscillation of the power system [13, 14]. Usually, the WADC is designed based on the constant active power control loop of VSC-HVDC to suppress the oscillation by adjusting the active power injected into the AC system [15, 16]. Since the active and reactive power of VSC-HVDC are decoupling and adjustable, it

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is supposed to make full use of the controllability to design the dual-loop (the active and reactive power control loops) WADC, for the sake of better performance on suppressing the oscillation and improving the stability of power system.

In general, there are two kinds of methods for designing WADCs, including model-based method and data-driven method. For the former one, the conventional wide-area damping controller (C-WADC) is designed under the specific operating condition using the linearization model of the system, which has the poor adaptability to the change of operating condition [17]. In this regard, the robust damping controllers [14, 18] are proposed to cope with different operating conditions of the concerned power system. However, the design of this kind of controllers usually needs the detailed mathematical model of the system, which is difficult to obtain for a practical power grid. The latter data-driven one does not require the mathematical model of the concerned system, which includes model-free adaptive control [19], artificial intelligent control [20, 21] and approximate dynamic programming (ADP) [22, 23]. Among them, ADP is a combination of optimal control, approximation function, and reinforcement learning and becomes a research hotspot recently [24]. Goal representation Heuristic Dynamic Programming (GrHDP) [25, 26], as one of the ADP algorithms, can generate the internal reinforcement signal to realize the online adaptation to the change of operating condition better than conventional ADP with external reinforcement signal. GrHDP has been used for the damping control in AC/DC hybrid transmission system [27] and the coordinated control of doubly fed wind turbine and STATCOM [28]. But there is no application in designing WADC for BTB-VSC-HVDC.

In addition, there is always a time delay in communication of wide area measurement signals. Many references do not consider the effect of time delay or regard it as a fixed value [29] during the design of WADC. However, the time delay is stochastic in fact due to the communication interference and channel congestion, which would deteriorate the control performance or even cause instability of the whole system [30, 31]. Generally, there are two main ways to deal with the stochastic communication delay. One is to design a controller with a certain delay tolerance capability [32], such as delay-dependent feedback controller [33, 34], H_∞ robust controller [35]. However, this kind of controllers cannot adequately eliminate the adverse effect of stochastic delay, and the tolerance range for time delay is relatively limited. The other is to design the controller with the ability to actively compensate the communication delays [36, 37, 38]. In [36], The bounded random time delay is divided into several intervals and compensators are designed for each time delay interval. Whereas, the design of the delay compensator needs to know the frequency of the concerned oscillation in advance. In [37], a robust controller with adaptive delay compensator is proposed to compensate the time delay without the prior knowledge of the frequency of the concerned oscillation.

This paper proposes a data-driven adaptive wide-area damping controller (D-WADC) for BTB-VSC-HVDC system based on the constant active and reactive power control loop. It is designed using GrHDP algorithm which can adapt to the change of system operating condition. At the same time, an adaptive delay compensator (ADC) is also introduced into the proposed D-WADC to compensate the stochastic communication time delays. Both simulation and hardware-in-loop experiment results of a simplified practical power system verified the effectiveness of the proposed D-WADC.

The main contributions of this paper are listed as follows:

- Considering the independent control of active and reactive power, a dual-loop D-WADC for BTB-VSC-HVDC is proposed to suppress the inter-area oscillation in power system, which is better than the conventional single-loop WADC in terms of damping performance.
- The D-WADC is designed based on GrHDP, which only needs the input and output data rather than the mathematic model of the concerned system. Thus, the D-WADC can always provide good performance by online weight modification under a wide-range of system operating condition and disturbances.
- An adaptive delay compensator (ADC) is also introduced to the D-WADC to effectively compensate both the fixed and stochastic delay existing in the wide-area signal in real time. Moreover, the ADC need neither the frequency information of concerned oscillation mode nor any model information of the system.
- Both the simulation and hardware-in-loop experiment results on a simplified practical grid and 16-machine power system verify that the proposed D-WADC can effectively suppress the low-frequency oscillation under a wide range of operating conditions, disturbances, and stochastic communication delays.

The rest of this paper is organized as follows. Section 2 briefly introduces the model and basic control structure of BTB-VSC-HVDC. Section 3 presents the detailed structure of the data-driven WADC. And section 4 gives the

design procedures of C-WADC and D-WADC. Simulation verifications on the simplified model of practical grid and the 16-machine power system are presented in section 5 and section 6, respectively. And the hard-in-loop experiment study is given in Section 7. Finally, the conclusions are drawn in section 8.

2. Model and Basic Control of BTB-VSC-HVDC

2.1. Model of BTB-VSC-HVDC

The BTB-VSC-HVDC technology is based on the pulse width modulation (PWM) technology and voltage source converter (VSC), as shown in Fig. 1. Generally, the basic control structure of BTB-VSC-HVDC can be divided into three layers: system-level control, station-level control, and valve-level control. As the key layer, the station-level control adopts cascaded control including the outer loop control and inner loop control. The outer loop control is used to realize the function of converter station, such as the constant direct current (DC) voltage U_{dc} control (marked as ①) and the constant AC voltage V_s control (marked as ②) at d axis, the constant active power P control (marked as ③) and the constant reactive power Q control (marked as ④) at q axis. The references of the outer loop control are given by the system-level control. And the current references generated by the outer loop control are fed into the inner loop control. The inner loop adopts the current decoupling control strategy, by which the independent control of active and reactive power is achieved. The output of the inner loop is fed into the valve-level control to generate the PWM signals for the IGBTs. The IGBTs are turned on and off according to the PWM signals, which achieves the commutation function of VSCs, rectifier and converter.

Although the function combination of the outer loop control is flexible, there is an inviolable principle for BTB-VSC-HVDC. That is, if a converter on one side adopts constant active power control, the converter on the other side must adopt constant DC voltage control. In this way, the DC voltage can maintain stability when BTB-VSC-HVDC tracks the active power transmission instruction. Thus, the practical strategies for BTB-VSC-HVDC could be ①②+③②, ①②+③④, ①④+③④ and ①④+③②, which makes it suitable for different applications such as asynchronous interconnection [39], renewable energy integration [40, 41, 42], and weak grid power supply.

In this paper, the rectifier of the BTB-VSC-HVDC adopts constant DC voltage control and constant AC voltage control, while the inverter adopts constant active power control and constant reactive power control. And the schematic diagram of BTB-VSC-HVDC is shown in Fig. 1.

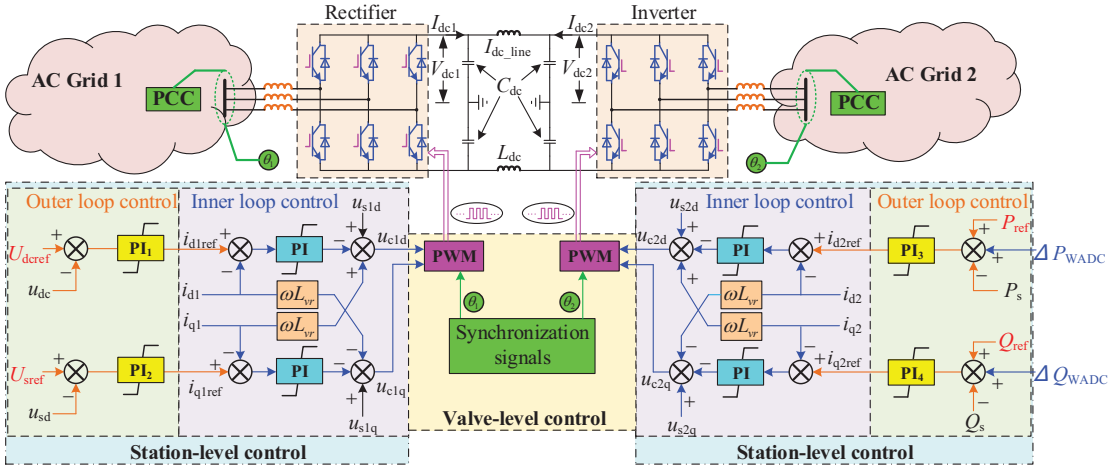


Figure 1: Schematic diagram of the basic control for BTB-VSC-HVDC

2.2. Outer Loop Control

As shown in Fig. 1, the PI control structure is utilized for the outer loop control of the rectifier and inverter. In detail, the constant DC voltage control is formulated as [43],

$$i_{d1\mathrm{ref}} = (k_{\mathrm{p1}} + \frac{k_{\mathrm{i1}}}{s})(U_{\mathrm{dcref}} - u_{\mathrm{dc}}) \tag{1}$$

the constant AC voltage control:

$$i_{q1\mathrm{ref}} = (k_{\mathrm{p2}} + \frac{k_{\mathrm{i2}}}{s})(U_{\mathrm{sref}} - u_{\mathrm{s}}) \tag{2}$$

the constant active power control:

$$i_{d2\mathrm{ref}} = (k_{\mathrm{p3}} + \frac{k_{\mathrm{i3}}}{s})(P_{\mathrm{ref}} - P_{\mathrm{s}} + \Delta P_{\mathrm{WADC}}) \tag{3}$$

the constant reactive power control:

$$i_{q2\mathrm{ref}} = (k_{\mathrm{p4}} + \frac{k_{\mathrm{i4}}}{s})(Q_{\mathrm{ref}} - Q_{\mathrm{s}} + \Delta Q_{\mathrm{WADC}}) \tag{4}$$

where u_{dc} and u_{s} represent the measured DC voltage on the DC link and the measured AC voltage at the point of common coupling (PCC), respectively. P_{s} and Q_{s} are the measured active and reactive power injected to AC grid, respectively. U_{dcref}, U_{sref}, P_{ref},and Q_{ref} are the reference of u_{dc}, u_{s}, P_{s},and Q_{s}, respectively. ΔP_{WADC} and ΔQ_{WADC} represent the supplementary active and reactive power reference provided by WADC. $i_{d1\mathrm{ref}}$ and $i_{q1\mathrm{ref}}$ respectively represent the reference value of the inner loop current components at d and q axis of rectifier, while $i_{d2\mathrm{ref}}$ and $i_{q2\mathrm{ref}}$ represent that of inverter. $k_{\mathrm{p}j}$ and $k_{\mathrm{i}j}$, $j = 1,2,3,4$ represent the proportional and integral parameters of these outer loop control structures.

3. Data-driven Adaptive Wide-Area Damping Control Structure

Fig. 2 shows the control structure of D-WADC which is attached to the control cabinet of VSC as a supplementary controller for the basic control structure. Once the wide-area measurement signal is received, D-WADC firstly uses ADC to compensate the communication delay in real time and then generates a parallel phase shift signal with the phase shifting unit (PSU). Together with the delay compensated signal and its phase shifting signal, D-WADC finally outputs the real-time control signal by the GrHDP neural networks. Note that the adaptability of the proposed D-WADC has two layers of meaning: one is that the ADC can adaptively compensate the stochastic delay; the other refers to the adaptability to the change of operating condition, which is achieved by the GrHDP network.

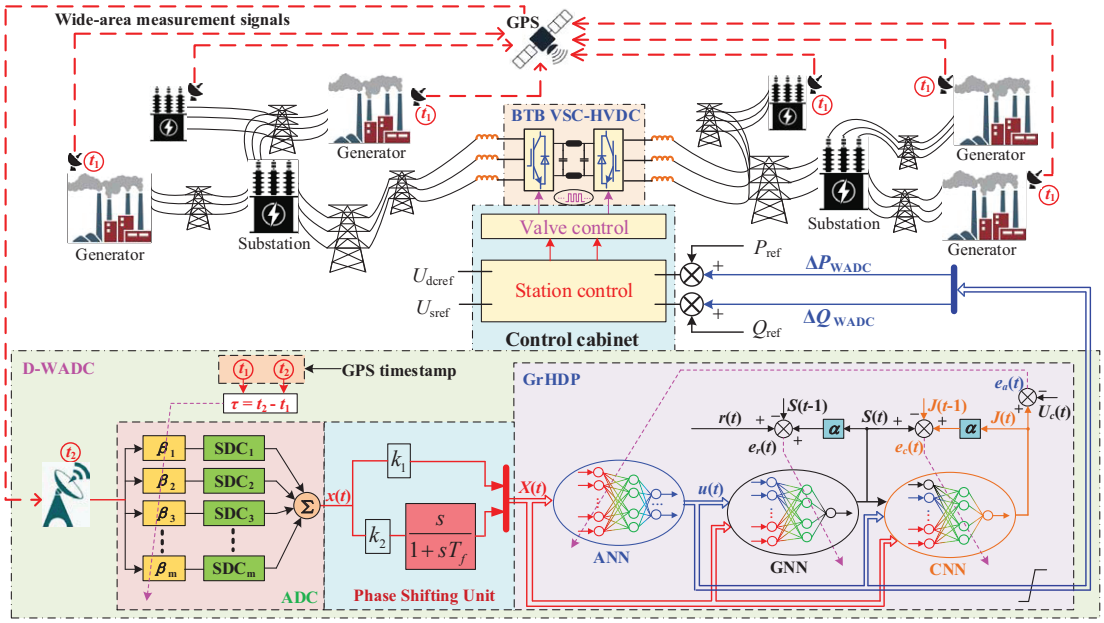


Figure 2: Structure of data-driven wide-area damping control

3.1. Adaptive Delay Compensator

A phase lag will be introduced into the wide-area signal by the communication delay, which reduces the control effectiveness of WADC. Moreover, the delay of the wide-area signal will be stochastic due to the communication interference and channel congestion. The conventional fixed-delay compensator is not able to deal with the stochastic delay effectively. Thus, it is necessary to adopt the ADC which can compensate the stochastic delay of the wide-area signals.

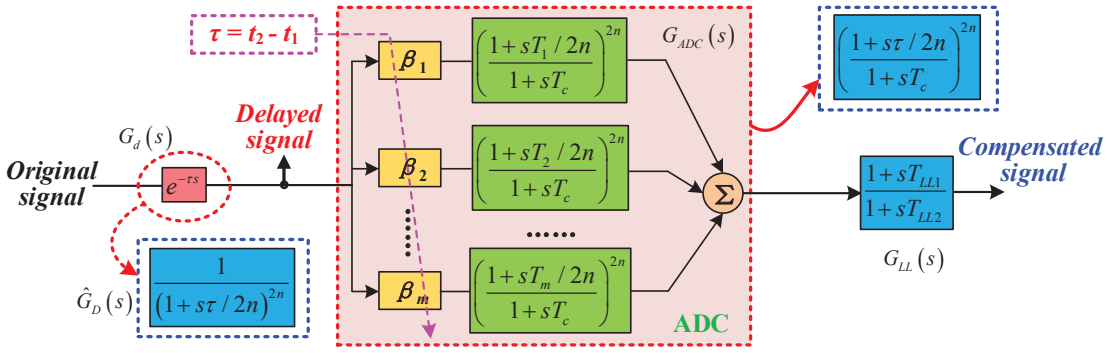


Figure 3: Structure of adaptive delay compensator

Considering that the Global Position System (GPS) provides the unified time stamps for both the phase measurement unit (PMU) and the WADC, the delay of the wide-area signal can be calculated in real time. As shown in Fig. 3, t_1 and t_2 represent the measuring time at PMUs and the receiving time at WADC, respectively. Then the delay of the current signal data is $\tau = t_1 - t_2$ and the corresponding model can be expressed as:

$$G_d(s) = e^{-\tau s} = (e^{-\frac{\tau s}{n}})^n \tag{5}$$

where n is a positive integer. The communication delay can be approximately represented by the *Pade* approximation. Due to the sufficiently small approximation error and relatively small computational complexity, the first order *Pade* approximation is applied for $e^{-\frac{\tau s}{n}}$ and the approximate delay model is given by:

$$G_D(s) = (\frac{1-\frac{s\tau}{2n}}{1+\frac{s\tau}{2n}})^n = \frac{((1-\frac{s\tau}{2n})(1+\frac{s\tau}{2n}))^n}{(1+\frac{s\tau}{2n})^{2n}} = \frac{(1-(\frac{s\tau}{2n})^2)^n}{(1+\frac{s\tau}{2n})^{2n}} \tag{6}$$

Note that the approximate model is only used in the design of ADC. When it comes to the time domain simulation or real-time experiment, the exact model of communication delay is used to verify the delay compensation effect. To illustrate the ADC design principle, a transfer function with the same denominator as (6) is defined as follows:

$$\widehat{G}_D(s) = \frac{1}{(1+\frac{s\tau}{2n})^{2n}} \tag{7}$$

According to the bode diagram of (6) and (7), the phase of $G_D(s)$ is accurately similar to the phase of $\widehat{G}_D(s)$. That is to say, once the ADC compensate for the phase lag caused by $\widehat{G}_D(s)$, it just effectively compensate for the phase lag caused by $G_D(s)$, and further $G_d(s)$.

As shown in Fig. 3, the ADC is composed of a series of weighted sub-delay compensators (SDC). The transfer functions of ADC and SDC are expressed as follows:

$$G_{ADC}(s) = \sum_{i=1}^{m} \beta_i(\tau) G_{SDC_i}(s) \tag{8}$$

$$G_{SDC_i}(s) = (\frac{1+\frac{sT_i}{2n}}{1+sT_c})^{2n}, i = 1, 2, ..., m \tag{9}$$

where m is the number of SDC. β_i and T_i represent the weight and time constant of the i-th SDC. For the sake of good compensation effect, T_i is pre-designed and supposed to be between the minimum and the maximum delay. T_c is also the time constant of SDCs which is usually in the range of [0.01 s,0.1 s] considering the system dynamic characteristics [37].

In order to compensate the phase lag caused by $\widehat{G}_D(s)$, we make the numerator of $G_{ADC}(s)$ equal to the denominator of $\widehat{G}_D(s)$. That is,

$$\sum_{i=1}^{m} \beta_i(\tau)(1+\frac{sT_i}{2n})^{2n} \equiv (1+\frac{s\tau}{2n})^{2n} \tag{10}$$

From (10), the weight β_i can be calculated in real time according to:

$$\begin{bmatrix} \beta_1 \\ \beta_2 \\ \beta_3 \\ \vdots \\ \beta_m \end{bmatrix} = \begin{bmatrix} T_1^0 & T_2^0 & T_3^0 & \cdots & T_m^0 \\ T_1^1 & T_2^1 & T_3^1 & \cdots & T_m^1 \\ T_1^2 & T_2^2 & T_3^2 & \cdots & T_m^2 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ T_1^{m-1} & T_2^{m-1} & T_3^{m-1} & \cdots & T_m^{m-1} \end{bmatrix}^{-1} \begin{bmatrix} \tau^0 \\ \tau^1 \\ \tau^2 \\ \vdots \\ \tau^{m-1} \end{bmatrix} \tag{11}$$

where $m = 2n+1$. It conveys that β_i only depends on τ, since T_i is prior for the calculation. Therefore, the transfer function of the delay model together with ADC can be represented as:

$$\widehat{G}_D(s)G_{ADC}(s) = \frac{1}{(1+\frac{s\tau}{2n})^{2n}} \frac{(1+\frac{s\tau}{2n})^{2n}}{(1+sT_c)^{2n}} = \frac{1}{(1+sT_c)^{2n}} \tag{12}$$

In (12), the phase lag of the wide-area signal compensated by ADC is only related to T_c instead of the delay τ. And the phase shift caused by time constant T_c within the frequency band of low frequency oscillation, [0.2Hz, 2.5Hz], can be easily compensated by a lead-lag compensator. As shown in Fig. 3, it is given by,

$$G_{LL}(s) = \frac{1+sT_{LL1}}{1+sT_{LL2}} \tag{13}$$

where T_{LL1} and T_{LL2} are the time constants of the lead-lag compensator. As a result, the phase lag of the wide-area signal due to the communication delay can be almost eliminated. That is to say, ADC can realize the compensation of stochastic communication delay by online computing and adjusting the weights of SDCs, thus ensures the control effectiveness of D-WADC. Note that neither the mathematical model of the concerned system nor the exact frequency of the concerned oscillation mode is needed for the design of ADC. The communication delay is only considered in the wide-area signal fed into the WADC since the WADC is deployed on the converter of BTB-VSC-HVDC and the control signal does not need communication.

3.2. GrHDP Based Damping Control

3.2.1. Structure and Optimal Objective of GrHDP

As shown in Fig. 2, GrHDP adopts the three neural network structure, including action neural network (ANN), critic neural network (CNN) and goal neural network (GNN). All the three networks use the feedforward three-layer neural network, including the input layer, the hidden layer and the output layer.

For ANN, the input $X(t)$ is the wide-area signal, which can reflect the characteristics of the concerned oscillation mode. And the output $u(t)$ is the control signal applied to the concerned system, which represents the supplementary active power reference $\Delta P_{\mathrm{WADC}}(t)$ and reactive power reference $\Delta Q_{\mathrm{WADC}}(t)$.

For GNN, $r(t)$ represents the external reinforcement learning signal, which guides the weight modification of ANN and CNN in conventional approximate dynamic programming. The input signal of GNN is composed of $X(t)$ and $u(t)$. And the output signal is the internal reinforcement learning signal $S(t)$, which can optimize the mapping relationship between $X(t)$ and $u(t)$. It has been proven that $S(t)$ has the better adaptability to the change of operating condition than $r(t)$ [25].

For CNN, the input is composed of $X(t)$, $u(t)$ and $S(t)$, while the output is $J(t)$ called cost function. The optimization goal of the GrHDP algorithm is exactly to solve the following Bellman Equation.

$$J[x(i),i] = \sum_{i=1}^{\infty} \alpha^{t-i} U[X(t),u(t),t] \tag{14}$$

$$J^*[X(t)] = \min_{u(t)} U[X(t),u(t),t] + \alpha J^*[X(t+1)] \tag{15}$$

where U and α represent the utility function and the discount factor, respectively. α is less than 1. The solution of (14) is a set of optimal control signal $u(t)$, which can reduce $J(t)$ to the minimum $J^*(t)$. For a low frequency oscillation suppression problem, the utility function requires to reflect the oscillation intensity. And the optimal $J^*(t)$ can be set to 0, which means the goal of the control is to suppress the oscillation. The theoretical analysis of the convergence of the performance index and the existence of the admissible control are provided in [26]. Detailed information about the GrHDP refers to [25].

3.2.2. *Phase Shifting Unit of D-WADC*

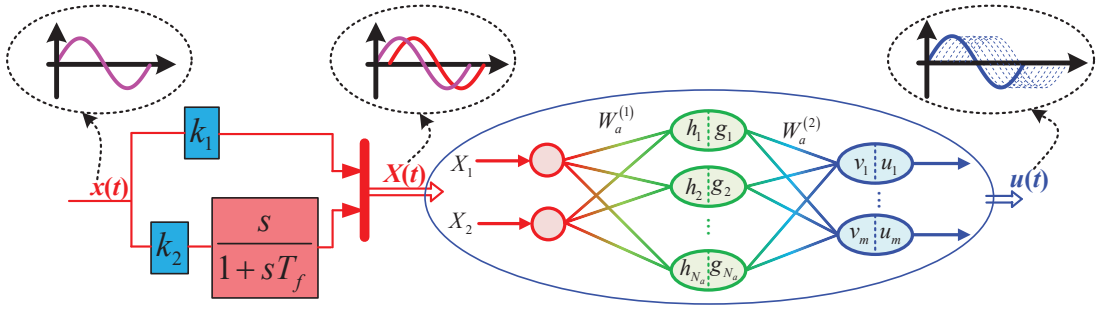


Figure 4: Structure of Phase Shifting Unit and Action Neural Network

As shown in Fig. 4, ANN generates and outputs the control signal $u(t)$, which is achieved by the following approximate function [25]:

$$\begin{aligned} u_k(t) &= \frac{1-e^{-v_k(t)}}{1+e^{-v_k(t)}} \quad v_k(t) = \sum_{j=1}^{N_a} W_{jk}^{(2)} g_j(t) \\ g_j(t) &= \frac{1-e^{-h_j(t)}}{1+e^{-h_j(t)}} \quad h_j(t) = \sum_{j=1}^{n} W_{ij}^{(1)} X_i(t) \end{aligned} \tag{16}$$

where $X_i(t)$ represents the i-th neuron in the input layer. $h_j(t)$ and $g_j(t)$ make up the j-th neuron in the hidden layer, while $v_k(t)$ and $u_k(t)$ make up the k-th neuron in the output layer. The approximate function of ANN is composed of the weighted sum function and the *Sigmoid* function, which is bounded and convenient to obtain the derivative. Hence, the data cannot diverge during the transmission in GrHDP.

However, there exists an obvious defect when calculating the damping control signals with (16). If the input wide-area signal $X(t)$ is zero, the output control signal $u(t)$ is necessarily zero. That means, the control signal generated by GrHDP cannot provide enough phase compensation for the input signal, which is important for damping control [44]. In this regard, the PSU is introduced into D-WADC to provide a parallel phase-shifting signal for ANN [27]. As shown in Fig. 4, T_f is the time constant of PSU. k_1 and k_2 are the gain constants to normalize the wide-area signal and the phase shifting signal. In this way, ANN can flexibly compensate the phase of the input signal with the weight modification and suppress the low frequency oscillation more effectively.

3.2.3. *Weight Modification of Neural Networks*

The weights of neural networks need modification and update to adapt to the change of system operating condition. Back propagation algorithm and gradient descent method are utilized for weight modification. The calculation rules of network errors are as follows [25]:

$$e_a(t) = J(t) - U_c(t) \quad E_a(t) = \tfrac{1}{2}e_a^2(t) \tag{17}$$

$$e_c(t) = \alpha J(t) - [J(t-1) - S(t)] \quad E_c(t) = \tfrac{1}{2}e_c^2(t) \tag{18}$$

$$e_g(t) = \alpha S(t) - [S(t-1) - r(t)] \quad E_g(t) = \tfrac{1}{2}e_g^2(t) \tag{19}$$

where $E_a(t)$, $E_c(t)$, $E_g(t)$ are the errors of ANN, CNN and GNN, respectively. $U_c(t)$ represents the optimal objective function value $J^*(t)$. Since the goal of damping control is to suppress the oscillation, $U_c(t)$ is supposed to be 0.

The rules of weight modification are as follows [25]:

$$\Delta W_{aij}^{(1)}(t) = -l_a(t)\frac{\partial E_a(t)}{\partial W_{aij}^{(1)}(t)} \quad \Delta W_{ajk}^{(2)}(t) = -l_a(t)\frac{\partial E_a(t)}{\partial W_{ajk}^{(2)}(t)} \tag{20}$$

$$\Delta W_{cij}^{(1)}(t) = -l_c(t)\frac{\partial E_c(t)}{\partial W_{cij}^{(1)}(t)} \quad \Delta W_{cjk}^{(2)}(t) = -l_c(t)\frac{\partial E_c(t)}{\partial W_{cjk}^{(2)}(t)} \tag{21}$$

$$\Delta W_{gij}^{(1)}(t) = -l_g(t)\frac{\partial E_g(t)}{\partial W_{gij}^{(1)}(t)} \quad \Delta W_{gjk}^{(2)}(t) = -l_g(t)\frac{\partial E_g(t)}{\partial W_{gjk}^{(2)}(t)} \tag{22}$$

In (20), $W_{aij}^{(1)}$ and $W_{ajk}^{(2)}$ represent the weights from input layer to hidden layer and the weights from hidden layer to output layer of ANN, respectively. And $l_a(t)$ is the learning rate of ANN. In (21), $W_{cij}^{(1)}$ and $W_{cjk}^{(2)}$ represent the weights from input layer to hidden layer and the weights from hidden layer to output layer of CNN, respectively. And $l_c(t)$ is the learning rate of CNN. In (22), $W_{gij}^{(1)}$ and $W_{gjk}^{(2)}$ represent the weights from input layer to hidden layer and the weights from hidden layer to output layer of GNN, respectively. And $l_g(t)$ is the learning rate of GNN.

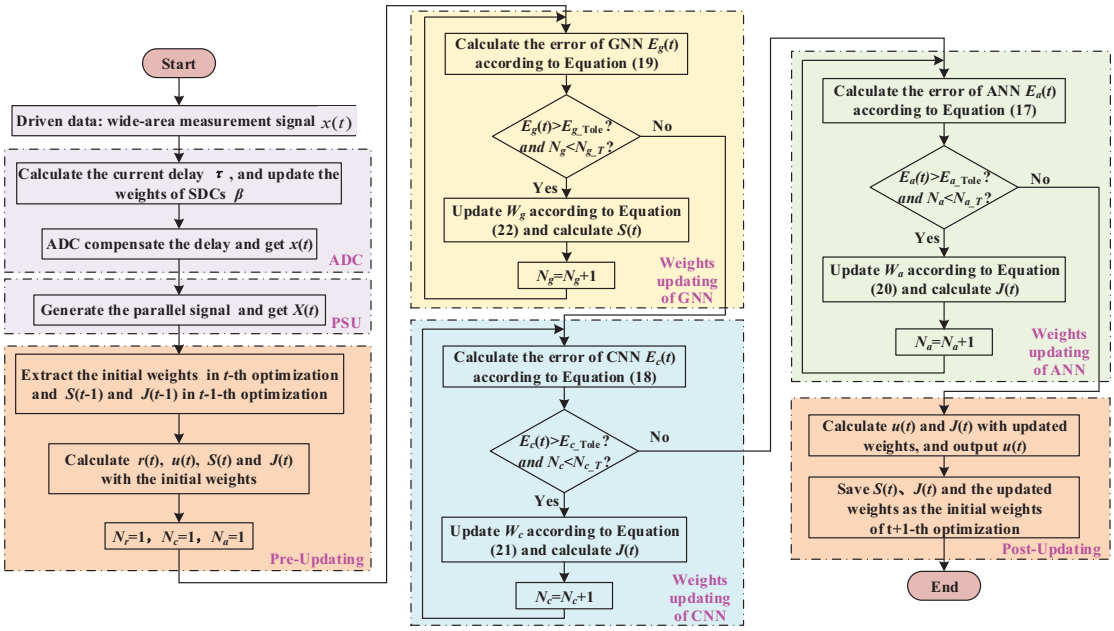


Figure 5: Flow chart of offline training and online learning for network weights of D-WADC

3.3. Training and Learning for D-WADC

Fig. 5 shows the offline training and online learning process of D-WADC. That the D-WADC receives a set of sample data of wide-area signal and generates the corresponding output control signals one time is called an optimization. In Fig. 5, E_{a_Tole}, E_{c_Tole}, and E_{g_Tole} represent the error tolerance of ANN, CNN, and GNN, respectively. Once the network error exceeds the corresponding tolerance, the weight modification begins. N_{a_T}, N_{c_T}, and N_{g_T} represent the upper limit of the iteration number of ANN, CNN, and GNN, respectively. When the iteration number exceeds the upper limit, the weight modification stops whether or not the network error is larger than the error tolerance. The upper limit of iteration is set to avoid excessive iteration in single optimization, which results in too long calculating time for the control signal and cannot meet the requirement of response speed.

As shown in Fig. 5, detailed steps of each optimization of D-WADC during the offline training and online learning are summarized as follows.

Step 1: Input the wide-area measuring signal $\widehat{x}(t)$, called driven data, and calculate the current communication delay τ and the corresponding weights of SDCs β.

Step 2: ADC updates β and compensates the communication delay. Then the compensated signal $x(t)$ is obtained.

Step 3: PSU is used to generate the parallel phase shift signal, and the compound signal $X(t)$ is obtained.

Step 4: Read $S(t-1)$, $J(t-1)$ and the initial weights of t-th optimization, and calculate $r(t)$, $u(t)$, $S(t)$, and $J(t)$.

Step 5: Calculate the error and modify the weights of GNN, CNN, and ANN in turn.

Step 6: Calculate $u(t)$, $S(t)$, and $J(t)$ with updated weights and output $u(t)$.

Step 7: Save $S(t)$, $J(t)$ and save the updated weights as the initial weights of next optimization.

Overall, GNN generates the internal reinforcement learning signal $S(t)$ and helps to update the weights of CNN, and CNN evaluates the utility of control signal and helps to update the weights of ANN. And ANN generates the optimal control signal with the updated weights.

Besides the weights modification during the online application of D-WADC, the offline training of network weights is also necessary, since the initial weights play an important role in control performance of D-WADC. As for the off-line training, the initial weights of neural networks are generated randomly and modified to adapt to the operating condition of the concerned system. The off-line simulation data and historical operation data under different operating conditions are utilized to train the networks to prevent the overtraining problem for a special scenario. The updated weights of neural networks will be used as the initial weights of the online application.

4. Design Procedure of the WADC

In order to verify the control performance of the proposed D-WADC, both the D-WADC and the conventional WADC (C-WADC) are designed for a simplified practical power system for comparison.

4.1. Test System Description

The National Power Grid Corp of China plans to build the Chongqing-Hubei BTB-VSC-HVDC to replace the AC transmission lines between Southwest Grid and Hubei Grid in 2018. This BTB-VSC-HVDC project uses 4 pairs of $\pm$420kV/1250MW converter, which has the highest voltage level and largest transmission capacity so far. For the convenience of simulation and real-time implementation, the two practical grids are simplified to 9 equivalent areas (EAs) including 9 equivalent generators and 8 equivalent loads. As shown in Fig. 6, all the equivalent generators are modeled with the 6th-order model and equipped with governors and excitation system, while all the equivalent loads adopt constant impedance model. Note that the oscillations occurred between different equivalent areas in the simplified system reflect the inter-area oscillations existed in the practical grid. Without losing generality, the simulation and experiment verifications are conducted aiming at the weakly damped oscillations in the simplified Hubei Grid.

There are four inter-area low frequency oscillation modes between different equivalent generators in different equivalent areas in Hubei Grid. And the damping ratios are 1.73%, 5.22%, 9.79%, and 7.17%, respectively, where only the first damping ratio is less than 5%. It is obvious that the first mode is weakly damped, which is the inter-area oscillation between EA5 and EA9 shown in Fig. 6. The frequency of the concerned mode is 1.2153Hz, which is a little higher than that of the normal inter-area mode due to the simplification of practical grids. To this end, a WADC could be designed on VSC to improve the damping of the concerned oscillation mode.

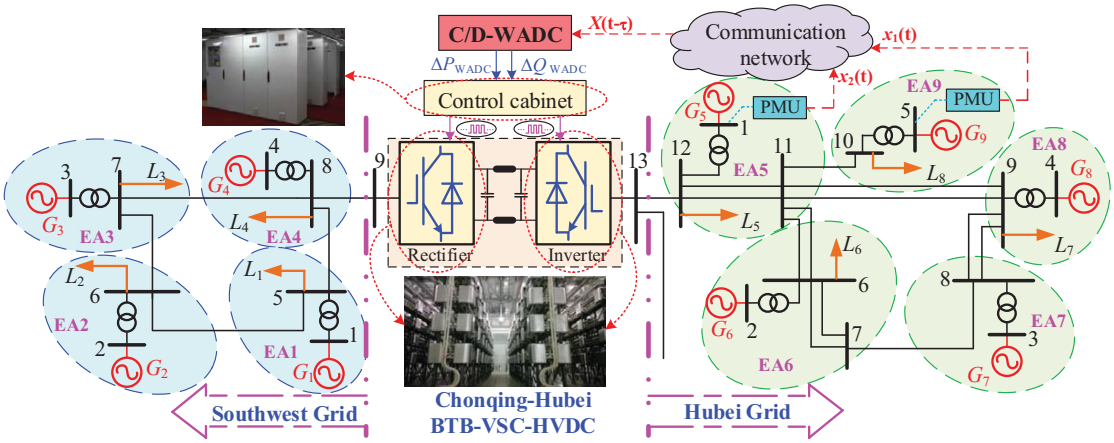


Figure 6: Simplified model of two AC systems interconnected by Chongqing-Hubei BTB-VSC-HVDC

4.2. Design of C-WADC

Based on the constant active and reactive power control loop, the C-WADC with lead-lag phase compensation structure is designed by means of the residue method [44]. The wide area measurement signal is carefully selected with the index of joint controllability/ observability measure (JCOM) [45]. The relative power angle between G_5 and G_9, $\Delta\delta_{5-9}$ is selected as the input signal of WADC, which has the relatively large JCOM of the concerned critical inter-area mode and relatively small JCOM of other modes so as to reduce interaction to other modes. And the output control signals of WADC are the supplementary active and reactive power reference of the inverter. The P-loop and Q-loop WADC are designed as follows:

$$\Delta P_{\mathrm{WADC}} = 5\frac{2s}{2s+1}\left(\frac{0.2583s+1}{0.0664s+1}\right)^2\Delta\delta_{5-9} \tag{23}$$

$$\Delta Q_{\mathrm{WADC}} = 5\frac{2s}{2s+1}\frac{0.1551s+1}{0.1104s+1}\Delta\delta_{5-9} \tag{24}$$

The damping ratio of the concerned mode reaches 10.68% when the dual-loop C-WADC is introduced here. As for the single-loop (P-loop and Q-loop) C-WADCs, they both improve the damping ratio slightly more than 5%. That means, compared with the single-loop C-WADCs, the dual-loop WADC can improve the damping of concerned mode more significantly. In addition, the damping ratios of the other modes existed in Hubei Grid are all more than 5% when different C-WADCs are added.

4.3. Design of D-WADC

The input signal collected for the design of D-WADC similarly needs to has large JCOM of the concerned critical inter-area mode. Such a signal can be selected through some data-driven methods, such as Multi-channel Continuous Wavelet Transformation (MCWT) [48] and Total least Square Estimation of Signal Parameter using Rotational Invariance Technique (TLS-ESPRIT) [49]. The larger the JCOM of the concerned mode the input signal has, the better control effect the WADC would get. In this paper, the input signal selected for the D-WADC is the same as that for C-WADC in order to guarantee the fairness of the control effect comparison between different WADCs.

For the design of ADC, assuming that the minimum and maximum communication delay of the practical power grid is 50 ms and 500 ms, the parameters of ADC are designed as follows: the number of SDC contained in ADC is $n = 2$, $m = 5$, and $T_1 = 0.1$ s, $T_2 = 0.2$ s, $T_3 = 0.3$ s, $T_4 = 0.4$ s and $T_5 = 0.5$ s. The fixed time constant is $T_c = 0.02$ s considering the system dynamic characteristic.

For the design of GrHDP networks, the hyper parameters are depicted in Table 1. Generally, the number of neuron in the GrHDP networks is designed by trial and error method or with reference to the principle given in [32]. The

Table 1: Parameters for networks of the D-WADC

Index	ANN	CNN	GNN
Input neurons	2	5	4
Hidden neurons	3	3	3
Output neurons	2	1	1
Learning rate	0.02	0.01	0.01
Iteration number	50	50	50
Error tolerance	10^{-8}	10^{-8}	10^{-8}
Weight range	± 5	± 5	± 5

parameters for PSU are set as: $k_1 = 6$, $k_2 = 0.9$, $T_f = 0.05$. Then, the input signal $X(t)$ is obtained as follow:

$$X(t) = \left[\Delta\delta_{5-9} \quad \frac{0.15s}{0.05s+1}\Delta\delta_{5-9}\right] \tag{25}$$

The outer reinforcement learning signal $r(t)$ is designed as follow:

$$r(t) = -(0.7x_1^2(t) + 0.3x_2^2(t)) \tag{26}$$

where $x_1(t)$ is the delay compensated wide-area signal and $x_2(t)$ is the parallel phase-shifting signal.

As for the initial weight parameters of GrHDP for online application, they are trained by the off-line simulation data of the concerned system. It is noted that the time consumed by one time weight modification is less than 1ms, which makes sure the D-WADC is rapid enough to adapt to fast transients during online application.

5. Simulation Verification of the Simplified System of Practical Grid

To verify the superiority of the proposed D-WADC, the following three kinds of simulations are conducted based on the test system under Matlab/Simulink environment. Firstly, the control performances of the dual-loop C-WADC under different disturbances are compared to that of single-loop C-WADC to verify the superiority of dual-loop WADC structure. Then, the control performances of C-WADC and D-WADC are compared under different scenarios, in order to verify the adaptability of the proposed D-WADC under a wide range of operating conditions. Finally, the ability of the proposed D-WADC compensating both the fixed and stochastic delays are also verified.

5.1. Case I: Dual-loop WADC and Single-loop WADC

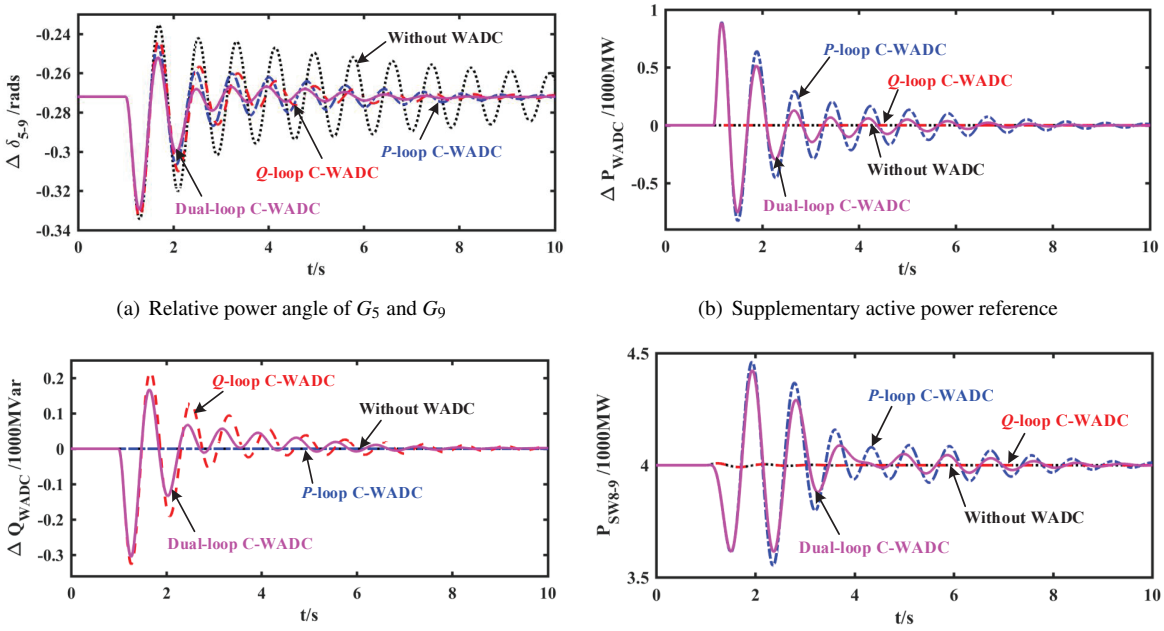
The control performance of dual-loop C-WADC and single-loop C-WADCs, including P-loop and Q-loop C-WADC, are compared under different contingencies listed in Table 2. There are 4 contingencies set for the comparison which are marked as $Sc.i$, $i = 1,2,3,4$. Fig. 7 gives the transient response of the test system with different C-WADCs under $Sc.2$, including the relative power angle of G_5 and G_9, $\Delta\delta_{5-9}$, the supplementary active and reactive power reference, ΔP_{WADC} and ΔQ_{WADC}, and the active power on line 8-9 in Southwest Grid, $P_{\mathrm{SW8-9}}$.

Table 2: Different contingencies set in Hubei Grid for superiority verification of dual-loop control structure

Scenarios	Contingencies
$Sc.1$	$t = 1s$, step increment of 2000 MW occurred to Load 5 at Bus 12.
$Sc.2$	$t = 1s$, a three-phase fault is applied in line 7-8 near bus 8 and tripped out at $t = 1.1s$, later the transmission line is reclosed successfully at $t = 2.1s$.
$Sc.3$	$t = 1s$, a three-phase fault is applied in line 8-9 near bus 9 and tripped out at $t = 1.1s$, later the transmission line is reclosed successfully at $t = 2.1s$
$Sc.4$	$t = 1s$, a three-phase fault is applied in line 6-7 near bus 7 and tripped out at $t = 1.1s$.

As shown in Fig. 7(a), the oscillation attenuates very slowly without C-WADC, while the oscillation can be suppressed in 10 s with C-WADCs. Moreover, the dual-loop C-WADC suppresses the oscillation more quickly than the single-loop (P-loop and Q-loop) C-WADC. Also, the ΔP_{WADC} required by dual-loop C-WADC is less than that of P-loop C-WADC and the ΔQ_{WADC} is less than that of Q-loop C-WADC, as shown in Fig. 7(b) and Fig. 7(c),

respectively. That is because the dual-loop control structure can make full use of both the decoupled active and reactive power injected to Hubei Grid, rather than one of them to suppress the oscillation. As a result, the dual-loop C-WADC can suppress the low frequency oscillation more efficiently than the single-loop C-WADCs.



(a) Relative power angle of G_5 and G_9

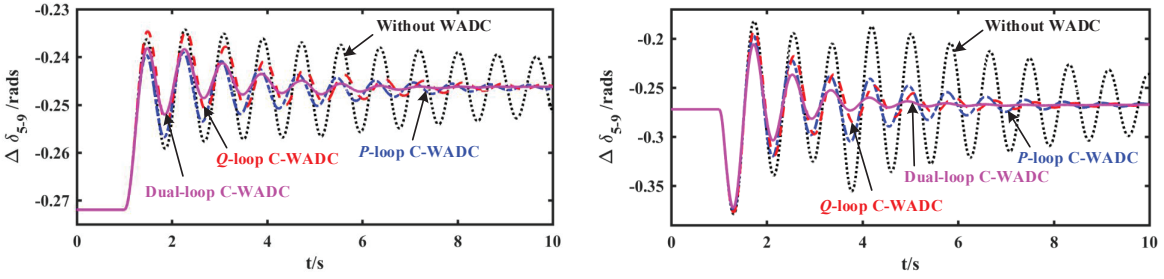
(b) Supplementary active power reference

(c) Supplementary reactive power reference

(d) Power on line 8-9 in Southwest Power Grid

Figure 7: Transient response characteristics of the disturbed system with different C-WADCs under Sc.2

In Fig. 7(d), the active power on line 8-9 $P_{\mathrm{SW8-9}}$ in Southwest Power Grid will hardly change with the Q-loop C-WADC or without WADC, but fluctuate with P-loop C-WADC and dual-loop C-WADC when Hubei Power Grid is disturbed. The reason is that the power transmitted by BTB-VSC-HVDC will change according to the supplementary active power reference during the post-fault transient response. That means the disturbance will be indirectly introduced into Southwest Grid. Fortunately and necessarily, it will be eliminated quickly as the low frequency oscillation in Hubei grid is quickly suppressed by WADCs, and the transient stability of the power system will be guaranteed. Compared with P-loop C-WADC, the disturbance in Southwest Grid is smaller and can be eliminated faster with dual-loop C-WADC since less ΔP_{WADC} is required.



(a) Relative power angle $\Delta\delta_{5-9}$ under Sc.1

(b) Relative power angle $\Delta\delta_{5-9}$ under Sc.4

Figure 8: Transient response characteristics with different C-WADCs under different scenarios

Fig. 8(a) and Fig. 8(b) show the control performances of different C-WADCs under *Sc*.1 and *Sc*.4. The results indicate that the dual-loop C-WADC performs better than single-loop C-WADCs in the situation of load mutation and

line out after permanent three-phase grounding faults.

Here, an integral of time multiplied by absolute error (ITAE) index [50] is defined as $J_{\mathrm{ITAE}} = \int_{t_1}^{t_2} t|e(t)|dt$. $t_1 = 1$s is the fault happening time, while $t_2 = 10$s is the simulation ending time. And $|e(t)|$ represents the absolute error between the transient value and the post-fault steady state value of $\Delta\delta_{5\_9}$. Since $\Delta\delta_{5-9}$ has large JCOM of the concerned critical inter-area mode, the J_{ITAE} index is well suited for quantitative assessment of the effectiveness of suppressing the concerned oscillation in time domain. Hence, the J_{ITAE} index is increasingly used to assess the damping control effect [27, 51]. Obviously, the smaller the J_{ITAE} is, the better the control performance is.

Fig. 9 shows the J_{ITAE} of different C-WADCs under different scenarios. The J_{ITAE} of dual-loop C-WADC is the smallest under all the scenarios listed in Table 2, followed by the single-loop C-WADCs which are roughly the same. That is to say, the dual-loop control structure shows the superiority to the single-loop control structure in suppressing the low frequency oscillation under different disturbances.

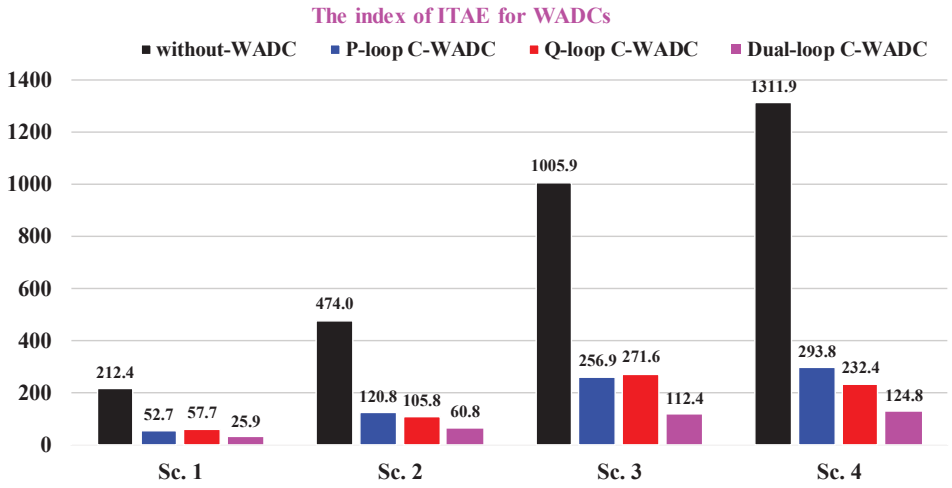


Figure 9: Control performance of different WADCs under different scenarios

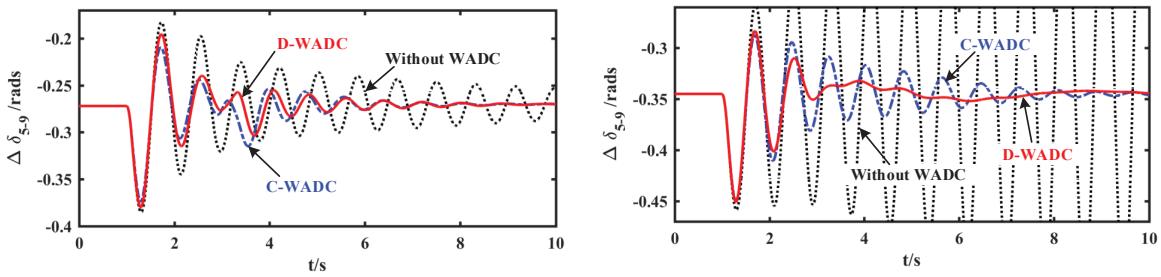
5.2. *Case II: Adaptability to Operating Conditions*

In order to verify the adaptability of the D-WADC to a wide range of operating conditions, two different scenarios under typical and changed operating conditions listed in Table 3 are simulated. The changed operating condition is obtained by adjusting the generation and active load in Hubei Grid according to the range of practical operation. The damping ratio of the concerned mode 1 under the changed operating condition is -1.88%, showing a negative damped state. Note that the communication delay is not considered in this simulation. The dual-loop C-WADC is also simulated to compare with the proposed D-WADC in the following simulations.

The transient response with different WADCs under *Sc*.I and *Sc*.II are compared respectively in Fig. 10. And Fig. 11 gives the internal variable of D-WADC under *Sc*.II, including the ANN network error E_a, the external reinforcement learning function $r(t)$, the internal reinforcement learning function $S(t)$, the cost function $J(t)$ and the ANN weights $W_a^{(1)}$ and $W_a^{(2)}$.

Table 3: The different contingencies set in Hubei Grid for superiority verification of D-WADC

Operating condition	Scenarios	Contingencies
Typical	*Sc*.I	A three-phase fault is applied in line 9-11 near bus 9 at $t = 1$ s. The faulty line is tripped out in 100 ms.
Changed	*Sc*.II	A three-phase fault is applied in line 7-8 near bus 8 at $t = 1$ s. The faulty line is tripped out in 100 ms and reclosed successfully in another 1 s.



(a) *Sc*. I: Typical Operating Condition (b) *Sc*. II: Changed Operating Condition

Figure 10: Transient performance after single disturbance under different scenarios

In Fig. 10(a), the low frequency oscillation can be quickly suppressed with C-WADC and D-WADC, and the control performances are roughly the same. It indicates that the proposed dual-loop D-WADC for BTB-VSC-HVDC based on GrHDP has the capability to suppress the low frequency oscillation . As shown in Fig. 10(b), the oscillation amplitude increases without WADC, since the concerned oscillation mode is negatively damped under the changed operating condition. Although the oscillation can still be suppressed with C-WADC, the control performance of D-WADC is obviously better than that of C-WADC. The reason is that the control parameters of C-WADC designed under the typical operating condition cannot change with the change of operating condition. Thus, the control performance of C-WADC will decrease when the system deviates from the typical operating condition. On the contrary, the proposed D-WADC trained under the typical operating condition can adapt to the change of operating condition by online weight modification, so as to maintain a excellent control effectiveness under different scenarios.

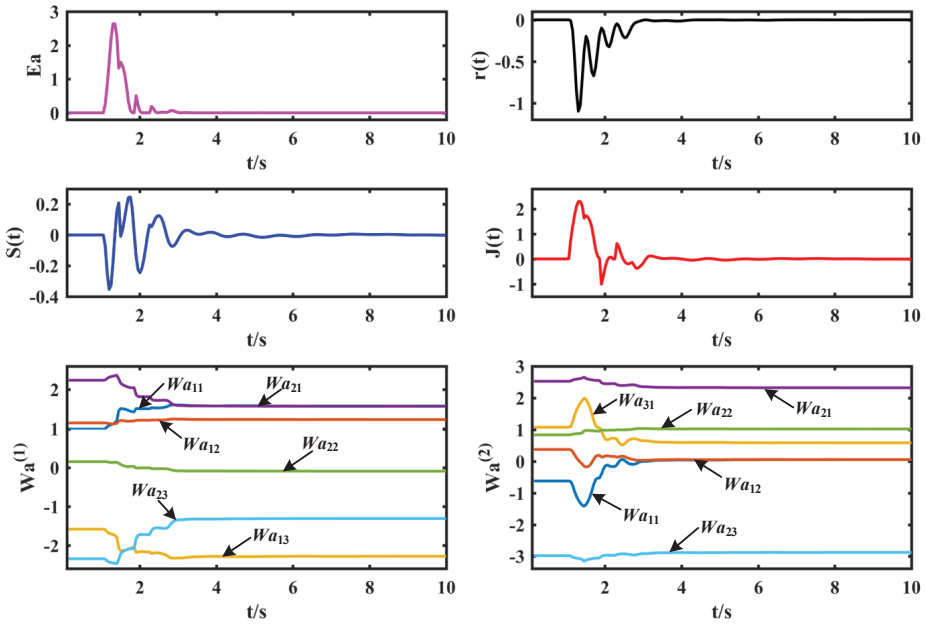


Figure 11: Inner variables of A-WADC under *Sc*. II

In Fig. 11, when the system is disturbed, the external reinforcement learning signal $r(t)$, the internal reinforcement learning signal $S(t)$ and the cost function $J(t)$ fluctuate correspondingly, which makes the ANN error Ea exceed the error tolerance value. Then the ANN begins to modify the weights $W_a^{(1)}$ and $W_a^{(2)}$ according to (20) with the help of CNN and GNN. And the output control signal of D-WADC is optimized with the weight modification. As the low

frequency oscillation is basically suppressed in about 4 s, the weights of ANN level off and D-WADC adapts to the changed operating condition. The results verify that the D-WADC can adapt to new operating conditions and different disturbances through weight modification.

5.3. Case III: Communication Delay Compensation

Different communication delays are considered to verify the delay compensation ability of D-WADC, including fixed delay, stochastic delay in a small range, and stochastic delay in a large range.

5.3.1. Fixed Delay

The operating condition and disturbance are the same as the *Sc*. II in Case II, and the fixed communication delay of 50 ms, 100 ms, and 150 ms are considered in this simulation. The transient response with different WADCs under different fixed delays are compared, and the corresponding J_{ITAE} are shown in Fig. 12.

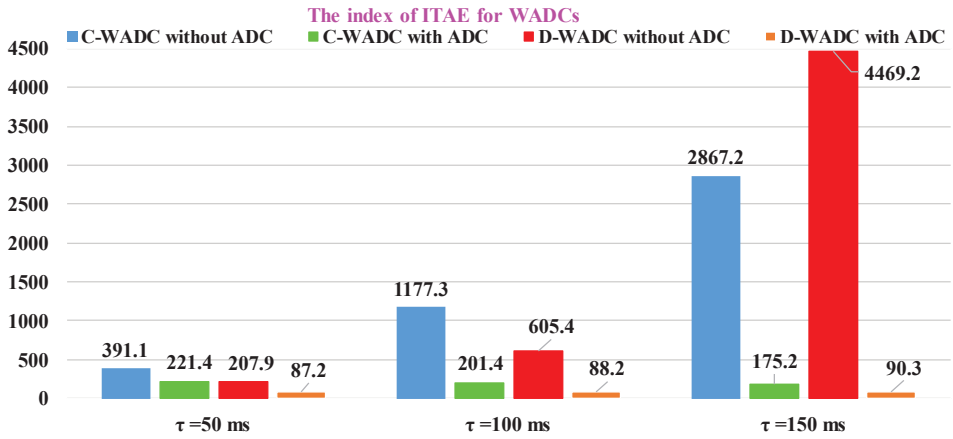


Figure 12: Control performance of different WADCs under different fixed time delays

In Fig. 12, the larger the fixed time delay is, the larger J_{ITAE} of C-WADC and the D-WADC without ADC are. Notice that the oscillation can still be suppressed by C-WADC and the D-WADC without ADC when the delay is $\tau = 50$ ms and $\tau = 100$ ms, which means they can tolerate time delays to a certain extent. However, when the delay reaches $\tau = 150$ ms, the J_{ITAE} of both the above WADCs increase rapidly, which means they can no longer suppress the oscillation in this situation. It concludes that the communication delay will worsen the control effectiveness of WADC and even deteriorate the transient stability of the concerned system. Meanwhile, it is noticed that the both the C-WADC and D-WADC with ADC keep small J_{ITAE} as the delay increases, while the J_{ITAE} of the proposed D-WADC with ADC is smaller than the other. That means the ADC unit can well compensate for the fixed communication delays.

5.3.2. Stochastic Delay in a Small Scale

The stochastic communication delays in small scale are set as: $\tau = 100 \pm 0$ ms (fixed time delay), $\tau = 100 \pm 20$ ms, $\tau = 100 \pm 40$ ms and $\tau = 100 \pm 60$ ms. The operating condition and fault are the same as *Sc*. II in Case II. Fig. 13 and Table 4 respectively show the control performance and the J_{ITAE} of the D-WADC with ADC under different stochastic delays. The corresponding weight modification of SDCs is given in Fig. 14.

Table 4: The J_{ITAE} under different stochastic delay in small scale

Delay(ms)	100	100 ± 20	100 ± 40	100 ± 60
J_{ITAE}	88.181	89.299	92.012	98.433

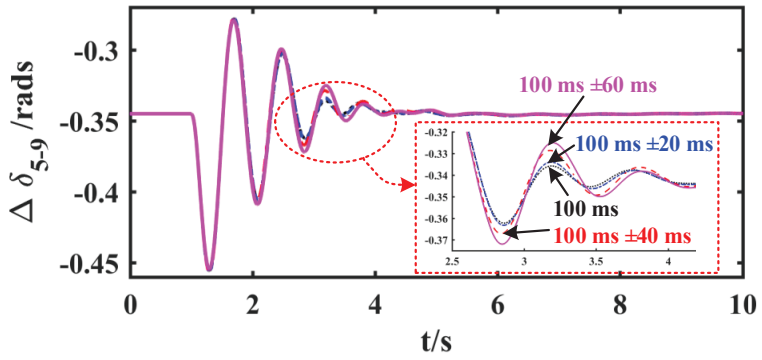


Figure 13: Control performance of D-WADC with ADC under different stochastic delay

As shown in Table 4 and Fig. 13, the J_{ITAE} increases with the expansion of the stochastic range of the delay and the control performance worsens slowly. However, the J_{ITAE} keeps a small value under these 4 situations. That means the proposed D-WADC has the ability to compensate for the stochastic time delay in a small range and suppress the low frequency oscillation very quickly.

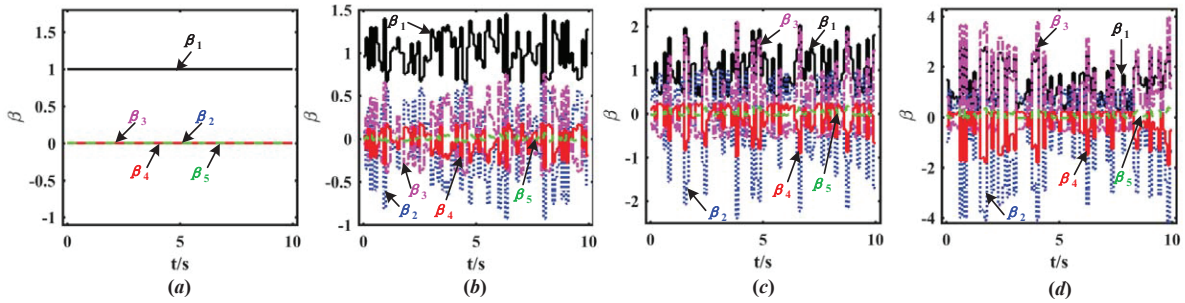


Figure 14: Weights of SDCs of ADC, (a)$\tau = 100 \pm 0$ ms, (b)$\tau = 100 \pm 20$ ms, (c)$\tau = 100 \pm 40$ ms, (d)$\tau = 100 \pm 60$ ms

In Fig. 14, when the stochastic range is 0, the weight of SDC1 β_1 is 1, and the weights of other SDCs is 0 since the foundation delay is 100 ms. As the stochastic range of the delay expands, the weight of SDC1 β_1 fluctuates near 1, and the weights of other SDCs fluctuate near 0. The larger the stochastic range is, the larger the amplitudes of the fluctuation are. It is the weight modification of SDCs that makes the ADC compensate the stochastic communication delay.

5.3.3. Stochastic Delay in a Large Scale

The operating condition and fault are the same as scenario II in Case II, and the stochastic range of communication delays are $\tau = 50 - 200$ ms, $\tau = 50 - 300$ ms, $\tau = 50 - 400$ ms and $\tau = 50 - 500$ ms, respectively. The post-fault transient response with different WADCs under different stochastic delays are compared. And the corresponding J_{ITAE} are shown in Fig. 15. Fig. 16 shows the $\Delta\delta_{5-9}$ with different WADCs under the delay of $\tau = 50 - 500$ ms and Fig. 17 gives the stochastic delay and corresponding weights of SDCs.

Fig. 15 shows that the J_{ITAE} generally increases with the expansion of the stochastic range of the delay, while the J_{ITAE} of the D-WADC with ADC keeps a small value. As shown in Fig. 16, without ADC, neither C-WADC nor D-WADC can suppress the oscillation under large-scale stochastic delay. As for C-WADC with ADC, it cannot suppress the oscillation either, even with the online weight modification of SDCs shown in Fig. 17. However, the proposed D-WADC with ADC can still suppress the low frequency oscillation quickly. That is because the ADC based on *Pade* approximation introduces an additional amount of amplitude distortion to the compensated signal under stochastic delay in large scale [38], which will influence the control performance of C-WADC. But the influence

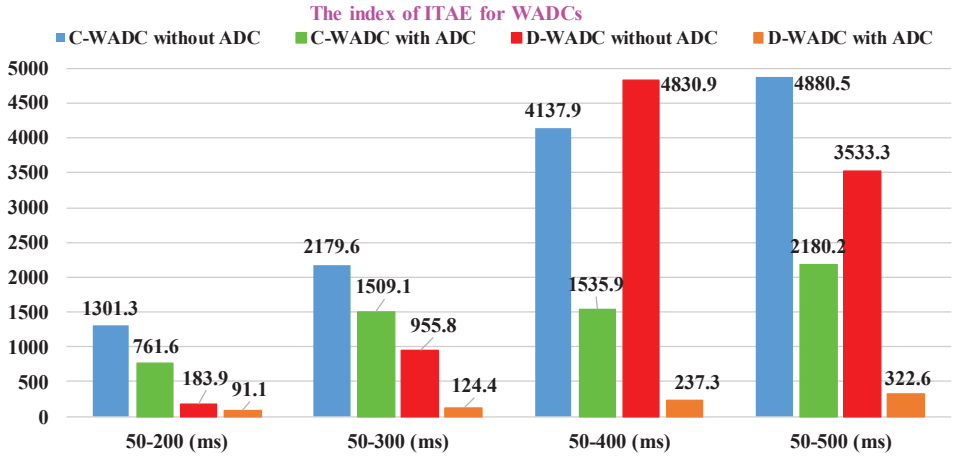


Figure 15: Control performance of different WADCs under different large-scale stochastic time delay

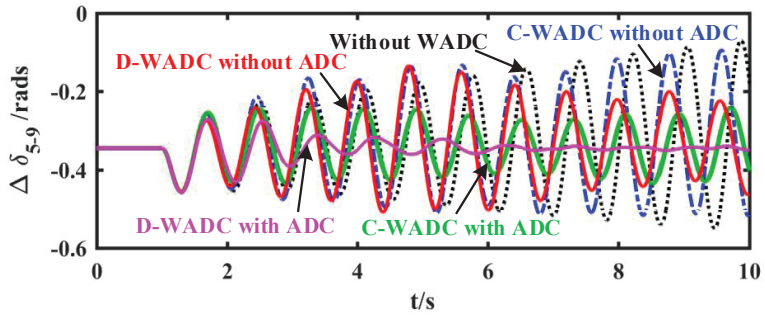


Figure 16: Control performance of different WADCs under stochastic time delay of 50 – 500 ms

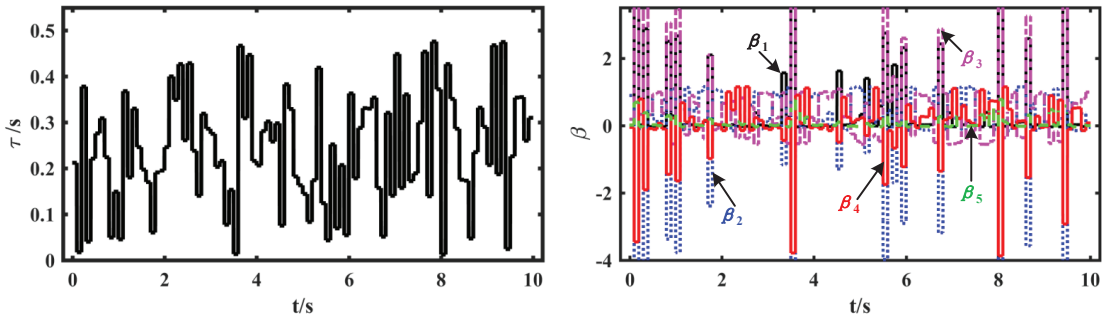


Figure 17: Stochastic delay within 50 – 500 ms and weights of ADC

can be eliminated immensely due to the online weight modification of GrHDP networks. That means the ADC can compensate the stochastic delay in a large range to some extent so that the proposed D-WADC can maintain the control effectiveness with the help of GrHDP.

6. Simulation Verification of IEEE 16-Machine System with BTB-VSC-HVDC

In order to verify the control effect of the D-WADC on the oscillation mode with different frequency, the simulation is also conducted on the IEEE 16-machine power system with BTB-VSC-HVDC. As shown in Fig.18, the BTB-VSC-HVDC with 10 pu rated power interconnects the bus 52 and the newly added bus 70. Power system stabilizers are installed for all generators, except for G13, G14, G15, and G16, to provide damping for local oscillation modes. The detail parameters of the 16-machine system refer to [45, 46, 47].

The modal analysis results show that there are 3 inter-area oscillation modes under typical operating condition, whose damping ratios are 9.68%, 17.15% and 2.17%. Obviously, the third mode is weakly damped, of which the oscillation frequency is 0.7446Hz. It is necessary to design a WADC to improve the damping of the concerned mode.

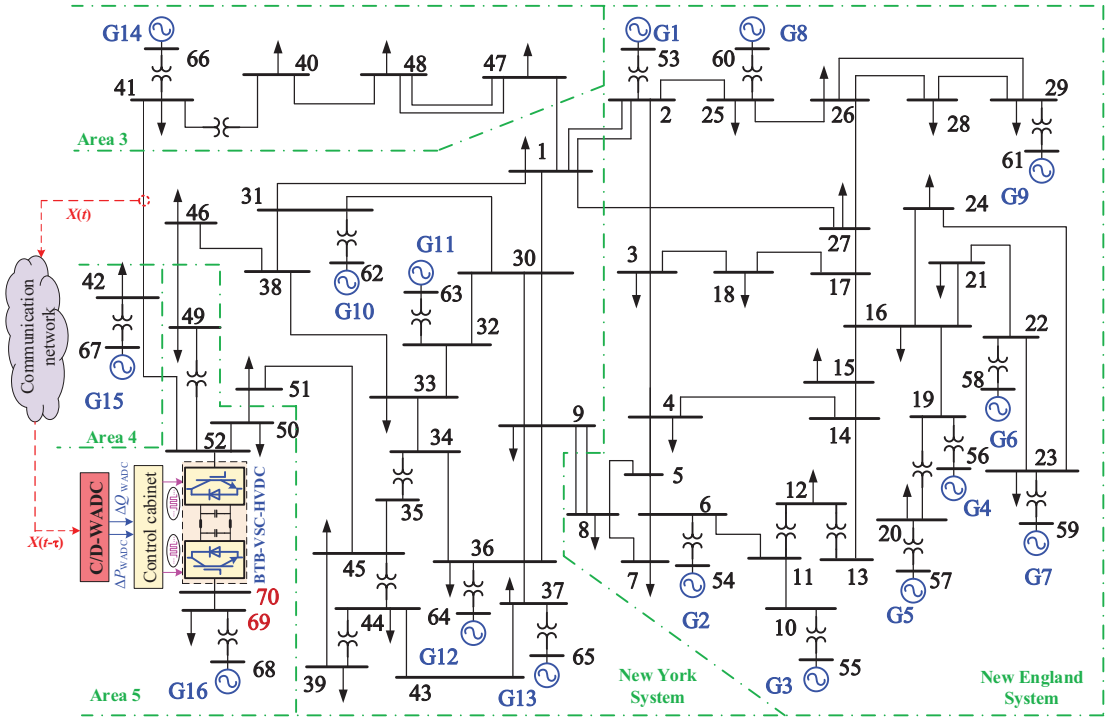


Figure 18: IEEE 16-Machine System with BTB-VSC-HVDC

As for the design of WADC, the active power transmitted on line 41-42, ΔP_{41-42}, with the largest JCOM of the concerned mode is selected as the input signal. And the dual-loop C-WADC is designed by the residue method as follows, which makes the damping ratio of the concerned mode increase to 9.97% under typical operating condition.

$$\Delta P_{\mathrm{WADC}} = 0.08\frac{2s}{2s+1}\left(\frac{0.5311s+1}{0.0860s+1}\right)^2\Delta P_{41-42} \tag{27}$$

$$\Delta Q_{\mathrm{WADC}} = 0.15\frac{2s}{2s+1}\left(\frac{0.5480s+1}{0.0834s+1}\right)^2\Delta P_{41-42} \tag{28}$$

For D-WADC, the parameters for ADC and GrHDP networks are the same as that in *Section* 4.3, while the parameters for PSU are set as: $k_1 = 1, k_2 = 0.15, T_f = 0.05$. Then, the input signal $X(t)$ is obtained as follow:

$$X(t) = \left[\Delta P_{41-42} \quad \frac{0.15s}{0.05s+1}\Delta P_{41-42}\right] \tag{29}$$

Note that the D-WADC designed for the concerned mode in 16-machine system also needs to be well trained offline before the online application.

Firstly, the simulation without delay is conducted under a changed operating condition, under which the damping ratio of the concerned mode with C-WADC installed decreases to 2.66%. A set of consecutive disturbances under the changed operating condition is given in Table 5. Fig. 19 shows the control performances of C-WADC and D-WADC and Fig. 20 shows the weight modification of ANN in D-WADC. As shown in Fig. 19, the D-WADC can suppress the oscillation more quickly the C-WADC, due to the weight modification of GrHDP networks shown in Fig. 20.

Table 5: Consecutive disturbances set in 16-machine system for superiority verification of D-WADC

Operating condition	Faulty time	Disturbance
Changed	$t = 1$s	A three-phase fault is applied in line 46-49 near bus 49. The faulty line is tripped out in 100ms and reclosed successfully in another 1s.
	$t = 15$s	A three-phase fault is applied in line 31-38 near bus 38. The faulty line is tripped out in 100ms.
	$t = 30$s	A step increment of 200MW occurred to the load at Bus 46.

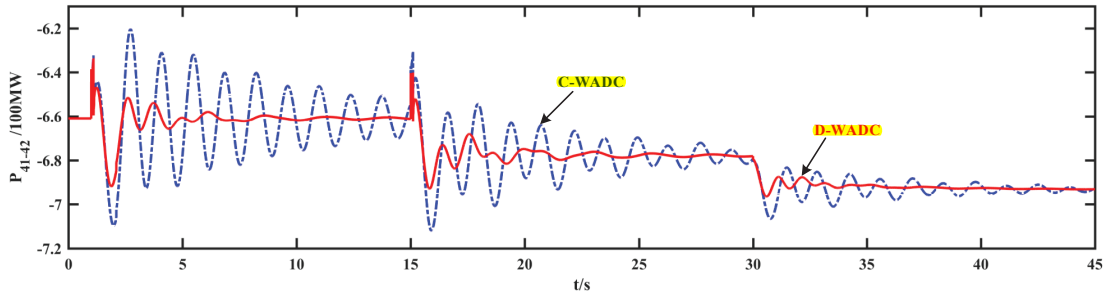


Figure 19: Transient performance under consecutive disturbances under the changed operating condition

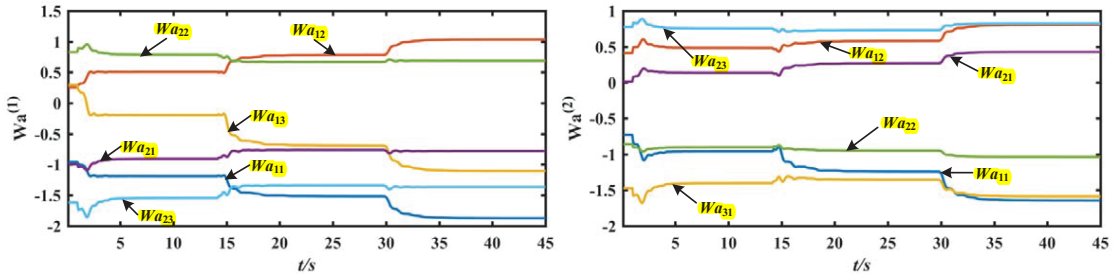


Figure 20: Weight modification of ANN in D-WADC

Then, the simulation under a stochastic communication delay, 50-500ms is conducted, and the disturbance is the first one listed in Table 5. Fig. 21 gives the control effects of different WADCs and Fig. 22 shows the communication delay and the corresponding weight modification of the ADC. As is shown in the two figures, only the D-WADC with ADC can suppress the low frequency oscillation quickly. The result indicates that the proposed D-WADC can effectively compensate for the stochastic delay with the weight modification of ADC.

7. Hard-In-Loop Experiment Studies

HIL has been identified as an significant and effective validation tool for the real-time implementation of new developed controllers and components in complex embedded system [52]. Compared with experiment using actual

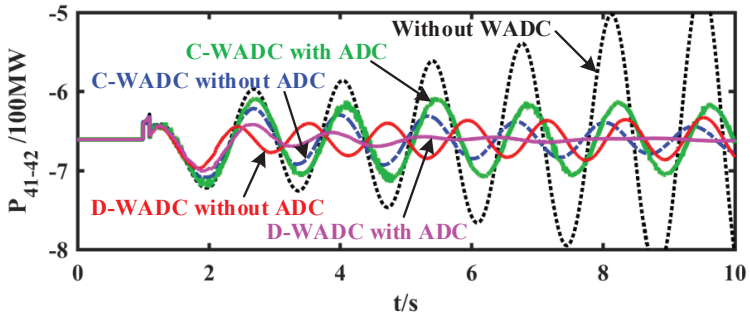


Figure 21: Control performance of different WADCs under stochastic time delay of 50 – 500 ms

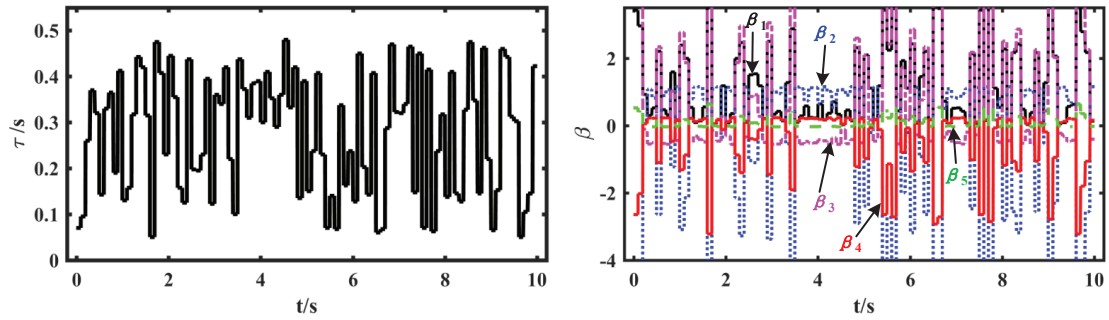


Figure 22: Stochastic delay within 50 – 500 ms and weights of ADC

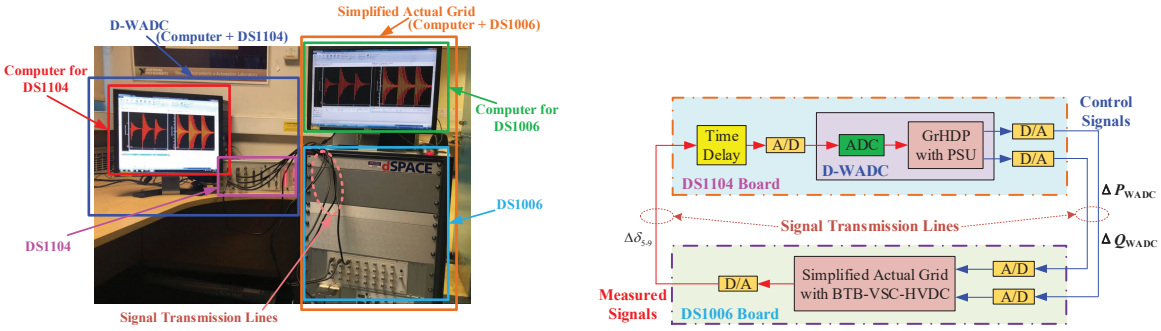
hardware, HIL experiment has the advantages of lower cost and less time to establish the experimental platform. Thus, it is usually undertaken to test and evaluate the effect of software and hardware in the early stage of controller development [53, 54, 55].

Here, a dSPACE based HIL experiment is conducted to verify the real-time control effectiveness of the proposed D-WADC. The configuration diagram and physical picture of the experimental platform are given in Fig. 23. As shown in Fig. 23(b), the D-WADC is simulated on DS1104 board with a sampling frequency $f_c = 500$ Hz, while the simplified actual grid with BTB-VSC-HVDC is simulated on DS1006 board with a sampling frequency $f_c = 1$ kHz. The measured signal $\Delta\delta_{5-9}$ is obtained from the real-time simulation of the simplified grid on the DS1006 board, which is sent to D-WADC implemented on the DS1104 board for the real-time control signals calculation. Then, the generated control signals ΔP_{WADC} and ΔQ_{WADC} are sent to the BTB-VSC-HVDC embedded in the DS1006 board to realize the close-loop control. The measured signal and control signals are transmitted via the signal transmission lines. Besides, the time delay unit is also embedded in DS1104 board, which makes it convenient to acquire the delay value τ.

7.1. HIL experiment I: Adaptability to Operating Conditions

In order to verify the online adaptability of D-WADC to operating conditions and disturbances, a set of consecutive disturbances under the changed operating condition as depicted in Section 5 is given in Table 6. Since the concerned mode is negatively damped under the changed operating condition, the transient response without WADC is expected to show the characteristic of divergent oscillation and not included in the comparison. The control performances of different WADCs (C-WADC and D-WADC) under the consecutive disturbances are shown in Fig. 24 and Fig. 25 gives one of the corresponding control signals ΔP_{WADC}. In addition, the weight modification of ANN in D-WADC is given in Fig. 26. Note that the time delay is not considered in this HIL experiment.

Figs. 24-25 convey that the D-WADC can successfully suppress the oscillation under multiple disturbances with better control performance than C-WADC. As shown in Fig. 26, the weights of ANN obviously changed when the



(a) Physical picture (b) Configuration diagram

Figure 23: Configuration diagram and physical picture of the experimental platform

Table 6: Consecutive disturbances set in Hubei Grid for superiority verification of D-WADC

Operating condition	Faulty time	Disturbance
Changed	$t = 1$ s	A three-phase fault is applied in line 7-8 near bus 8. The faulty line is tripped out in 100 ms and reclosed successfully in another 1 s.
	$t = 10$ s	A three-phase fault is applied in line 9-11 near bus 11. The faulty line is tripped out in 100 ms and reclosed successfully in another 1 s.
	$t = 20$ s	A three-phase fault is applied in line 8-9 near bus 9. The faulty line is tripped out in 100 ms and reclosed successfully in another 1 s.

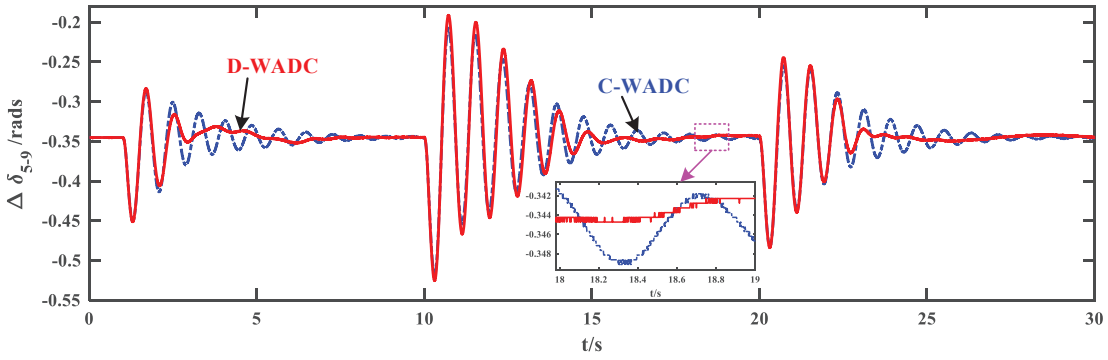


Figure 24: Transient performance under consecutive disturbances under the changed operating condition

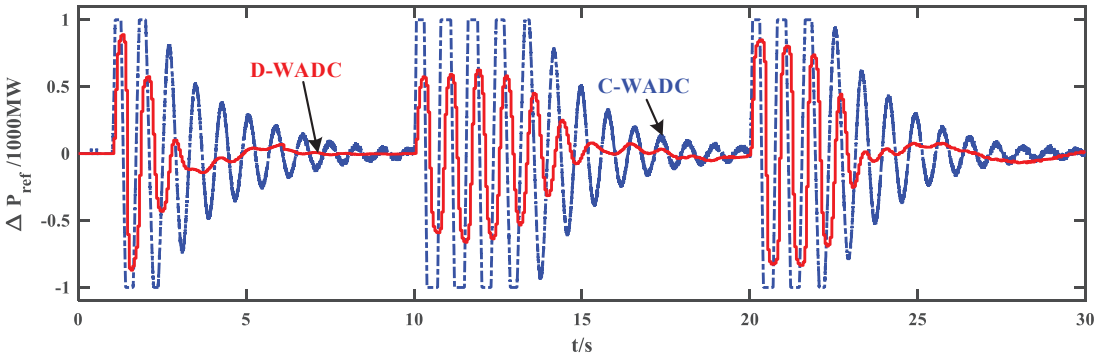


Figure 25: Control signal ΔP_{WADC} of different WADCs

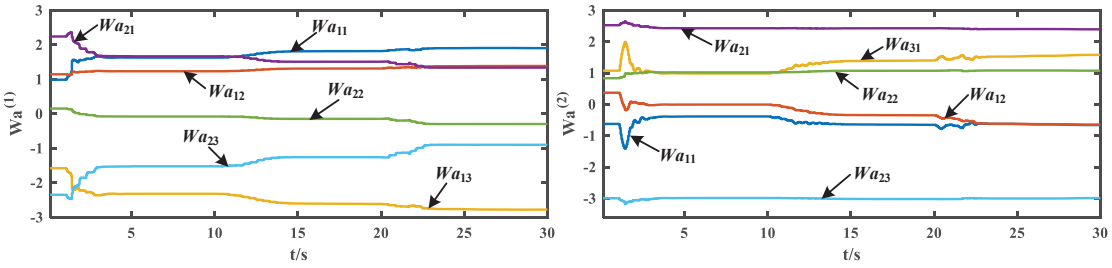


Figure 26: Weight modification of ANN in D-WADC

first disturbance occurred, which made the D-WADC adapt to the changed operating condition and suppressed the oscillation. The weights change slightly to optimize the output control signals to suppress the oscillation better during the following simulation. That means, the D-WADC can realize adaptability to operating conditions and disturbances through online weight modification during the real-time implementation.

7.2. HIL experiment II: Communication Delay Compensation

7.2.1. Fixed Delay

Under the same operating condition and disturbance as depicted in Section 5, Fig. 27(a) shows that the proposed D-WADC can suppress the oscillation effectively with fixed delay $\tau = 150$ ms. And the HIL experiment result is almost the same as that of the Matlab simulation.

7.2.2. Stochastic Delay in a Large Scale

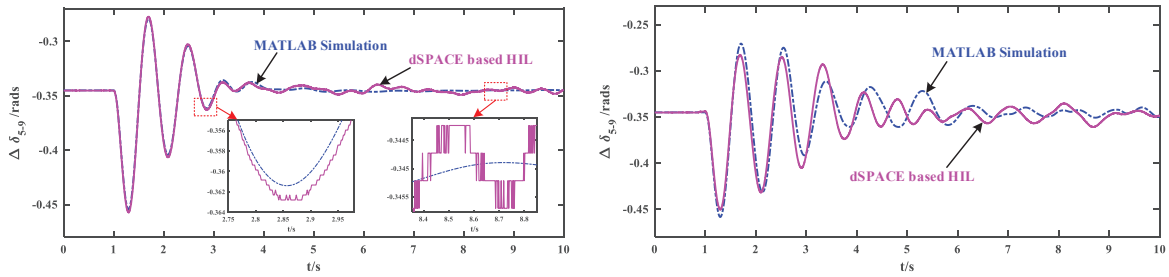
Under the same operating condition and disturbance as depicted in Section 5, Fig. 27(b) gives the result of HIL experiment under stochastic delay in a large scale. Note that the stochastic delay here is different from that shown in Fig. 17 in subSection 5.3.3, but the random ranges of both studies are the same, $\tau = 50 - 500$ ms. Though the result of HIL experiment cannot match that of Matlab simulation completely, it reveals that the D-WADC with ADC can compensate the stochastic delay and suppress the oscillation effectively.

The reasons for the slight difference between the HIL experiment results and simulation results are as follows:

- Compares with the Matlab simulation, there are some uncertain disturbances in measurements and noises during the signal transmission in the HIL experiment, which results in some unknown oscillation shown in Fig. 24 and Fig. 27(a) .
- The sampling frequency of DS1104 platform is different from that of Matlab simulation, which may introduce some additional error.
- For stochastic delay experiment, the main reason is that the two set of stochastic delay of HIL experiment and Matlab simulation are different, even though the stochastic range is the same.

7.3. Discussion

In general, the wide area measurement signal suffers from communication delay, data package loss and fake data. It is obvious that the data with poor quality would mislead the WADC to generate incorrect control signal and further deteriorate the control effect. Since the communication delay is the only data quality problem concerned in this paper, the data package loss and fake data should be avoided to the greatest possible during the real-time implementation. To this end, the dSPACE platform is required to keep supply reliable, connection solid, and electromagnetic compatible. Moreover, how to maintain the control effect of the data-driven WADC under the condition of false data or package loss will be investigated in our future work.



(a) Results under fixed delay $\tau = 150$ ms

(b) Results under stochastic delay $\tau = 50 - 500$ ms

Figure 27: Matlab Simulation and HIL experiment results of D-WADC with ADC under time delay

8. Conclusion

A data-driven adaptive wide-area damping controller of BTB-VSC-HVDC is proposed to suppress the inter-area low frequency oscillation under a wide range of operating conditions and different disturbances. The proposed D-WADC is designed based on the goal representation heuristic dynamic programming with a dual-loop control structure, which includes both the constant active and reactive power control loop of VSC. Also, the adaptive delay compensator is introduced into the proposed D-WADC to compensate the stochastic communication delay. Case studies are conducted on the simplified system of a practical power grid with Chongqing-Hubei BTB-VSC-HVDC and the 16-machine system with BTB-VSC-HVDC, respectively. The simulation results verify that the dual-loop control structure shows superiority over the single-loop one in damping improvement. Also, the GrHDP based D-WADC can adapt to a wide range of operating conditions and different disturbances through weight modification. Besides, the proposed D-WADC with ADC can compensate the fixed delay and stochastic delay to maintain the control effectiveness. Furthermore, the HIL experiment results validate the real-time implementation feasibility of the D-WADC. The proposed D-WADC has the potential to be applied in the coordinated wide-area damping control for different object (e.g., PSSs, photovoltaic, wind turbine, FACTs) with the consideration of communication delay, which can be included in future research works.

Acknowledgments

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